

IN THE CONFEED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Leonard Forbes et al.

Examiner:

Donghee Kang

Serial No.:

08/903,486

Group Art Unit:

2811

Filed:

July 29, 1997

Docket:

303.326US1

Title:

SILICON CARBIDE GATE TRANSISTOR

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENTE VED

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 NOV 0 6 2003

Technology Center 2100

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

11/05/2003 AADDF01 00000104 08903486

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Serial No :08/903486

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The Examiner is invited to contact the Applicants' Representative at the below-listed IVED telephone number if there are any questions regarding this communication.

NOV 0 6 2003

Respectfully submitted,

Technology Center 2100

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By their Representatives,

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Date 31 October 2003

Robert E. Mates Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this <u>3/5</u> day of October, 2003.

Signature

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	08/903486
(Use as many sheets as necessary)	Filing Date	July 29, 1997
	First Named Inventor	Forbes, Leon CEVED
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	Examiner Name	Kang, DongheeNOV 0 6 2003
Sheet 1 of 3	Attorney Docket No: 30	03.326US1 Technology Center 2100

	· · · · · · · · · · · · · · · · · · ·		ATENT DOCUMENT			
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,118,795	10/03/1978	Frye, R. C., et al.	365	222	08/27/1976
	US-4,384,349	05/17/1983	McElroy, D J.	365	185.02	06/02/1980
	US-4,598,305	07/01/1986	Chiang, A. , et al.	357	23.7	06/18/1984
	US-4,816,883	03/28/1989	Baldi, Livio	357	23.5	06/22/1987
	US-4,897,710	01/30/1990	Suzuki, A., et al.	357	71	08/18/1997
	US-4,980,303	12/25/1990	Yamauchi, T.	437	31	08/18/1988
	US-4,994,401	02/19/1991	Ukai, Y.	437	40	03/26/1990
	US-5,189,504	02/23/1993	Nakayama, S., et al.	257	422	01/30/1992
	US-5,317,535	05/31/1994	Talreja, Sanjay S., et al.	365	185	06/19/1992
	US-5,360,491	11/01/1994	Carey, P G., et al.	136	256	04/07/1993
	US-5,366,713	11/22/1994	Sichanugrist, P., et al.	423	346	05/28/1993
	US-5,388,069	02/07/1995	Kokubo, Masaya	365	185	03/18/1993
	US-5,409,501	04/25/1995	Zauns-Huber, R., et al.	8	94.29	07/06/1992
	US-5,424,993	06/13/1995	Lee, Roger R., et al.	365	218	11/15/1993
	US-5,425,860	06/20/1995	Truher, J. B., et al.	204	192.23	04/07/1993
	US-5,438,544	08/01/1995	Makino, Takami	365	185	01/28/1994
	US-5,441,901	08/15/1995	Candelaria, J.	437	31	06/10/1994
	US-5,467,306	11/14/1995	Kaya, Cetin , et al.	365	185.2	10/04/1993
	US-5,493,140	02/20/1996	Iguchi, Katsuji	257	316	06/21/1994
	US-5,623,160	04/22/1997	Liberkowski, J. B.	257	621	09/14/1995
	US-5,672,889	09/30/1997	Brown,	257	77	
	US-5,828,101	10/27/1998	Endo, K.	257	330	03/25/1996
	US-5,861,346	01/19/1999	Hamza, A., et al.	438	869	07/27/1995
	US-5,912,837	06/15/1999	Lakhani,	365	185.02	10/28/1996
	US-6,031,263	02/29/2000	Forbes, L., et al.	257	315	07/29/1997
	US-6,100,193	08/08/2000	Suehiro, S., et al.	438	685	09/24/1997
	US-6,307,775	10/23/2001	Forbes, L., et al.	365	185.01	08/27/1998
	US-6,309,907	10/30/2001	Forbes, L., et al.	438	108	08/21/1998
	US-6,365,919	04/02/2002	Tihanyi, J., et al.	257	77	07/11/2000

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T²
	JP-60-024678	02/07/1985	Akio, Nakatani	G06 K	9/36	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

EXAMINER

DATE CONSIDERED

Substitute for form 1449A/PTO
INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
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Sheet 2 of 3

Application Number	08/903486 DECEN/FD
Filing Date	08/903486 July 29, 1997 RECEIVED
First Named Inventor	Forbes, Leonard NOV 0 6 2003
Group Art Unit	2811
Examiner Name	Kang, Dongilechnology Center 210

Attorney	Docket	No:	303	.326	US′	ĺ
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Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BELTRAM, F., et al., "GaAlAs/GaAs Floating-Gate Memory Devices with	
		Graded-Gap Injector Grown by Molecular-Beam Epitaxy", IEEE Transactions on	
İ		Electron Devices, 35, Abstract No. VA-7,(Dec. 1988),2451	
		BELTRAM, F., et al., "Memory phenomena in heterojunction structures:	
		Evidence for suppressed thermionic emission", Appl. Phys. Lett., 53(5),	
		(1988),pp. 376-378	
		BOERINGER, DANIEL W., et al., "Avalanche amplification of multiple resonant	ļ
		tunneling through parallel silicon microcrystallites", Physical Rev. B, 51,	
		(1995),13337-13343	
		EDELBERG, E., et al., "Visible Luminescence from Nanocrystalline silicon films	
		produced by plasma enhanced chemical vapor deposition", Appl. Phys. Lett., 68,	
		(1996),1415-1417	
		HYBERTSEN, MARK S., "Absorption and Emission of Light in Nanoscale	İ
		Silicon Structures", Phys. Rev. Lett., 72, (1994),1514-1517	
		KATO, MASATAKA, et al., "Read-Disturb Degradation Mechanism due to	
		Electron Trapping in the Tunnel Oxide for Low-voltage Flash Memories", <u>IEEE</u>	
		Electron Device Meeting, (1994),45-48	
		LIN, B., et al., "Dramatic Reduction of Sidegating in MODFET's", IEEE	
		<u>Transactions on Electron Devices, 35, Abstract No. VA-6,(1988),pg. 2451</u>	
		LOTT, J., et al., "Anisotropic thermionic emission of electrons contained in	
		GaAs/AlAs floating gate device structures", Appl. Phys. Lett., 55(12), (1989),pp.	1
		1226-1228	
:		LOTT, J. A., et al., "Charge Storage in InAlAs/InGaAs/InP Floating Gate	
		Heterostructures", Electronics Letters, 26, (July 5, 1990),972-973	
		MOHAMMAD, S. N., et al., "Emerging Gallium Nitride Based Devices",	
		Proceedings of the IEEE, 83, (Oct. 1995),1306-1355	1
		NAKAMURA, J., et al., "CMOS Active Pixel Image Sensor with Simple Floating	
		Gate Pixels", <u>IEEE Transactions on Electron Devices</u> , 42, (1995),1693-1694	
		NEUDECK, P., et al., "Electrical Characterization of a JFET-Accessed GaAs	
		Dynamic RAM Cell", IEEE Electron Device Letters, 10(11), (1989),pp. 477-480	
		QIAN, Q., et al., "Multi-Day Dynamic Storage of Holes at the AIAs/GaAs	
		Interface", IEEE Electron Device Letters, EDL-7(11), (1986),pp. 607-609	
		RUSKA, W. S., "Microelectronic Processing", McGraw-Hill Book Co., (1987),281	
		SCHOENFELD, O., et al., "Formation of Si Quantum dots in Nanocrystalline	
-		silicon", Proc. 7th Int. Conf. on Modulated Semiconductor Structures, Madrid,	
-		(1995),605-608	
		SHARMA, B., et al., "Heterojunction Devices", In: Semiconductor	
_		Heterojunctions, Pergamon Press, New York, (1974), pp. 133-137	
-		STREETMAN, B., In: Solid State Electronic Devices, 4th Edition, Prentice Hall,	
1		New Jersey,(1995),pp. 217-219, 392-394	
		SZE, S. M., In: Physics of Semiconductor Devices, Wiley-Interscience, New	
		York,(1969),p. 496-497	

EXAMINER

DATE CONSIDERED

PTO/SB/08A(10-01)
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Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE STATEMENT BY APPLICANT **Application Number** 08/903486 July 29, 1997 (Use as many sheets as necessary) **Filing Date** Forbes, Leonard First Named Inventor NOV 0 3 2003 Technology Center 2100 **Group Art Unit** 2811 **Examiner Name** Kang, Donghee Attorney Docket No: 303.326US1 Sheet 3 of 3

	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		SZE, S. M., In: Physics of Semiconductor Devices. 2nd Edition, John Wiley & Sons, New York, (1981), pp. 122-129, 700-703, 708-710, 763-765	
		TSU, RAPHAEL, et al., "Slow Conductance oscillations in nanoscale silicon clusters of quantum dots", Appl. Phys. Lett., 65, (1994),842-844	
		TSU, R., et al., "Tunneling in Nanoscale Silicon Particles Embedded in an a-SiO2 Matrix", Abstract, IEEE Device Research Conference, (1996),pp. 178-179	
		WOLF, S., Silicon Processing for the VLSI Era, Vol. 3, Lattice Press, Sunset Beach, CA,(1995),311-312	
		YE, QIU-YI, et al., "Resonant Tunneling via Microcrystalline-silicon quantum confinement", Physical Rev. B, 44, (1991),1806-1811	
		ZHAO, X., et al., "Nanocrystalline Si: a material constructed by Si quantum dots", 1st Int. Conf. on Low Dimensional Structures and Devices, Singapore, (1995),467-471	